A 2.7GHz Phase Lock Loop in CMOS 0.18µm Technology

CMOS Analog Integrated Circuit Design
Course Project

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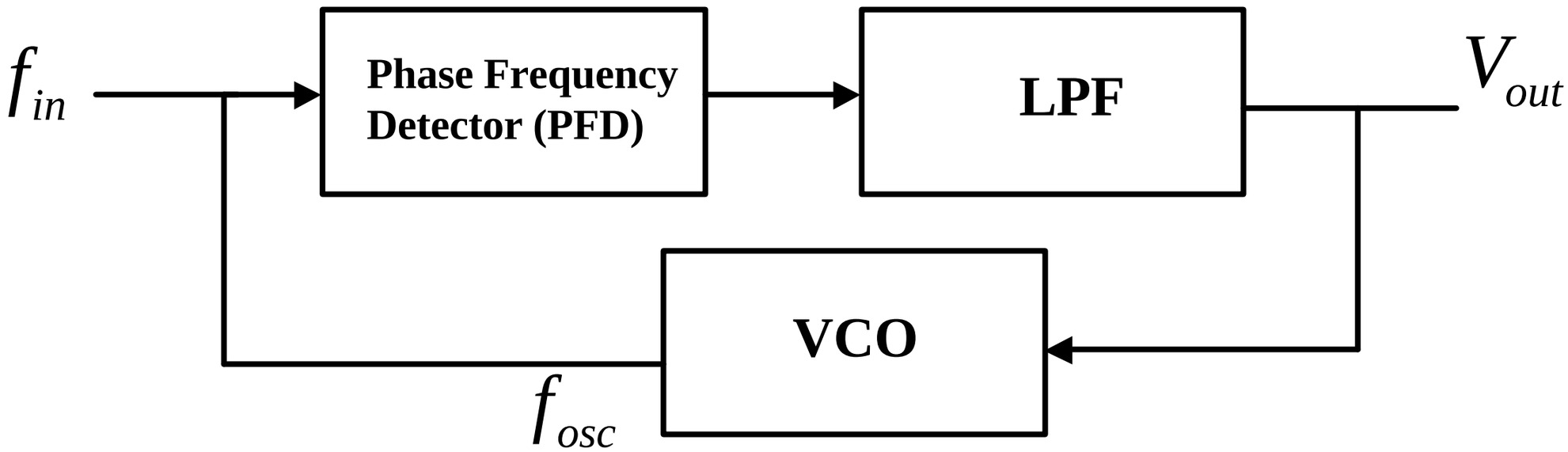
Functional block diagram of a typical PLL

The basic phase-locked loop circuit synchronizes an output signal with an input reference signal

The output signal has the same frequency as the input reference signal with a constant phase difference

Basic Phase-Locked Loop Architecture



PLL Applications

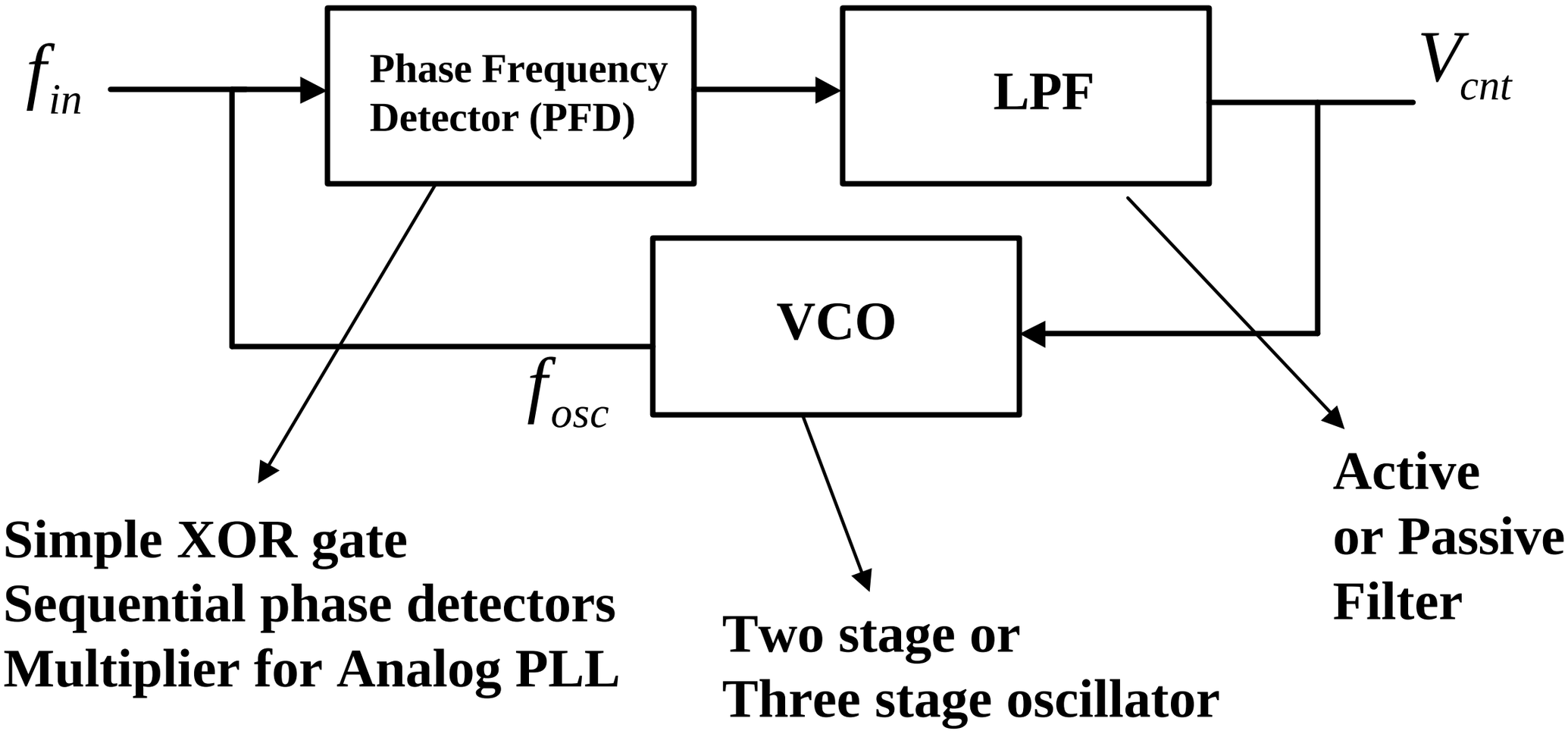
- **Clock Recovery**
  Regenerate Clock from input Data

  Tracking filter
  A narrow-band filter whose center frequency can move

- **Frequency Demodulation**
  FM demodulation

- **Frequency Synthesis**
  A frequency synthesizer generates multiples of an accurate reference frequency

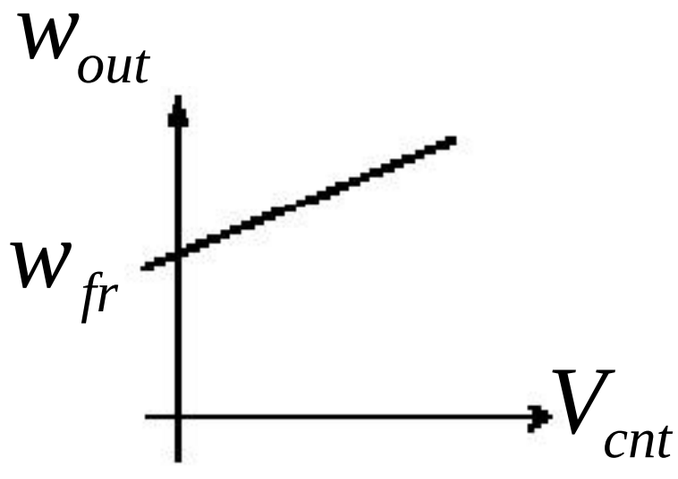
Building Blocks of Phase-Locked Loop

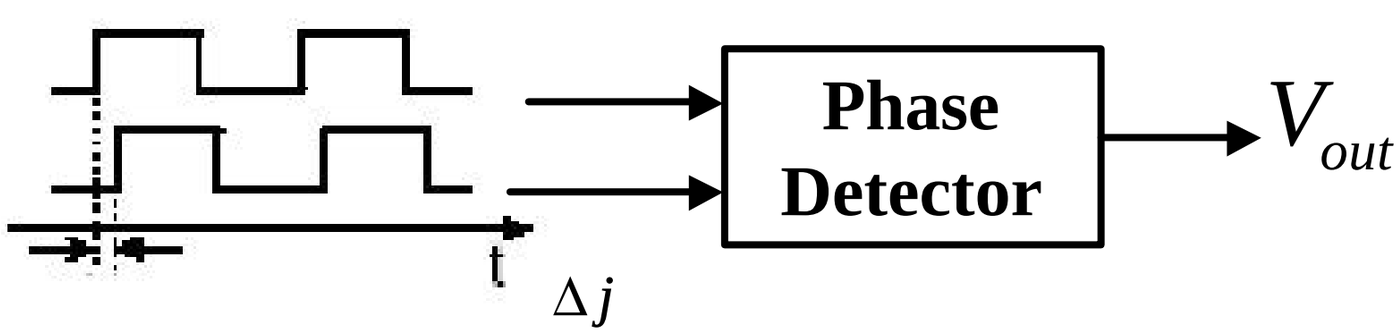


- Digital PLL uses logic gates to realize the phase detector
- Analog PLL uses a multiplier to implement the PD

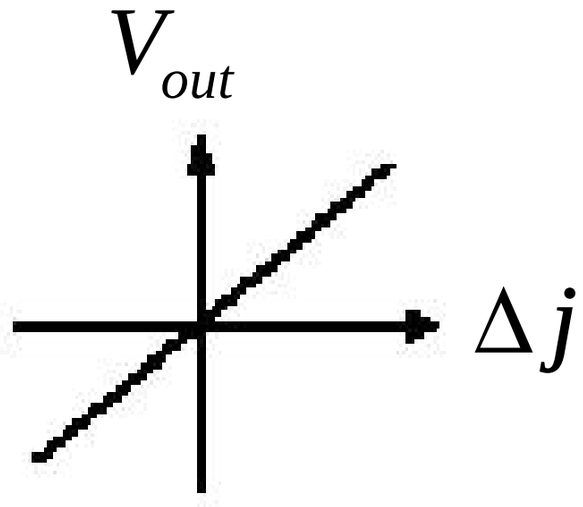
Dynamics of Building Blocks of PLL

$$w_{out} = w_{fr} + k_{vco} V_{cnt}$$



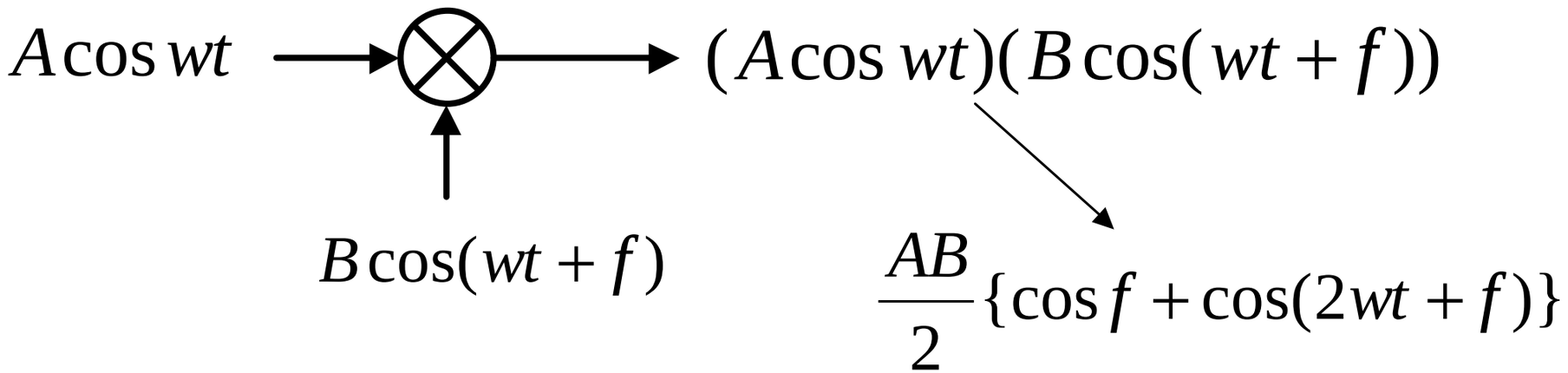


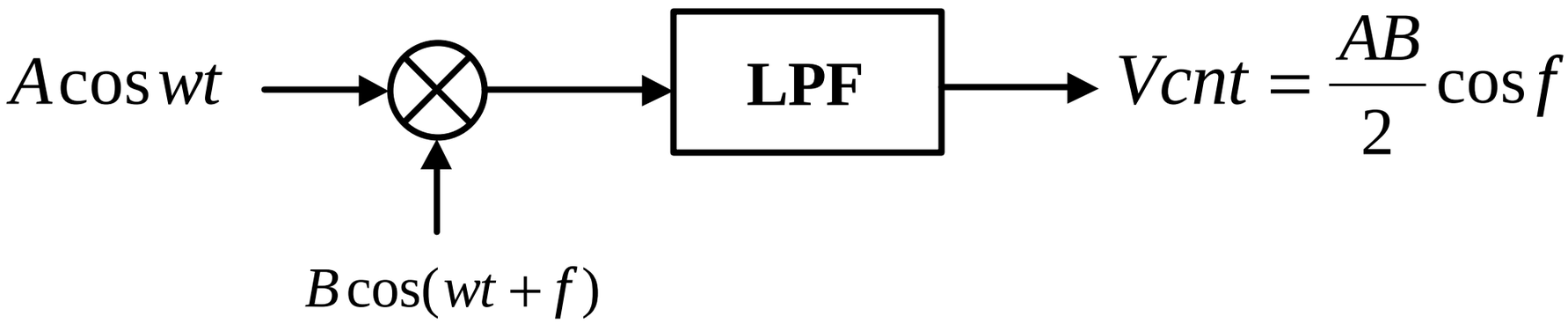
$$V_{out} = K_{pd} \Delta j$$



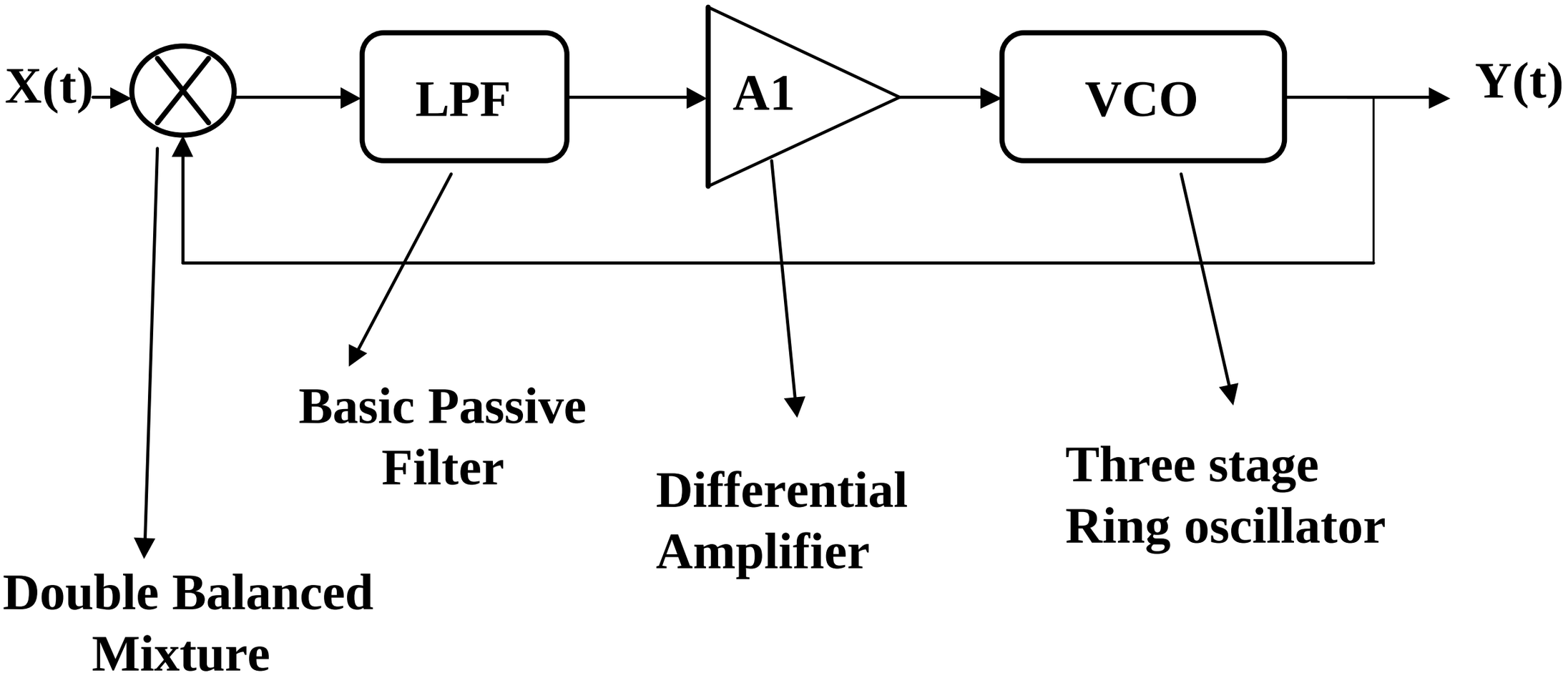
Dynamics of Building Blocks of PLL (continued)

Analog Phase Detector

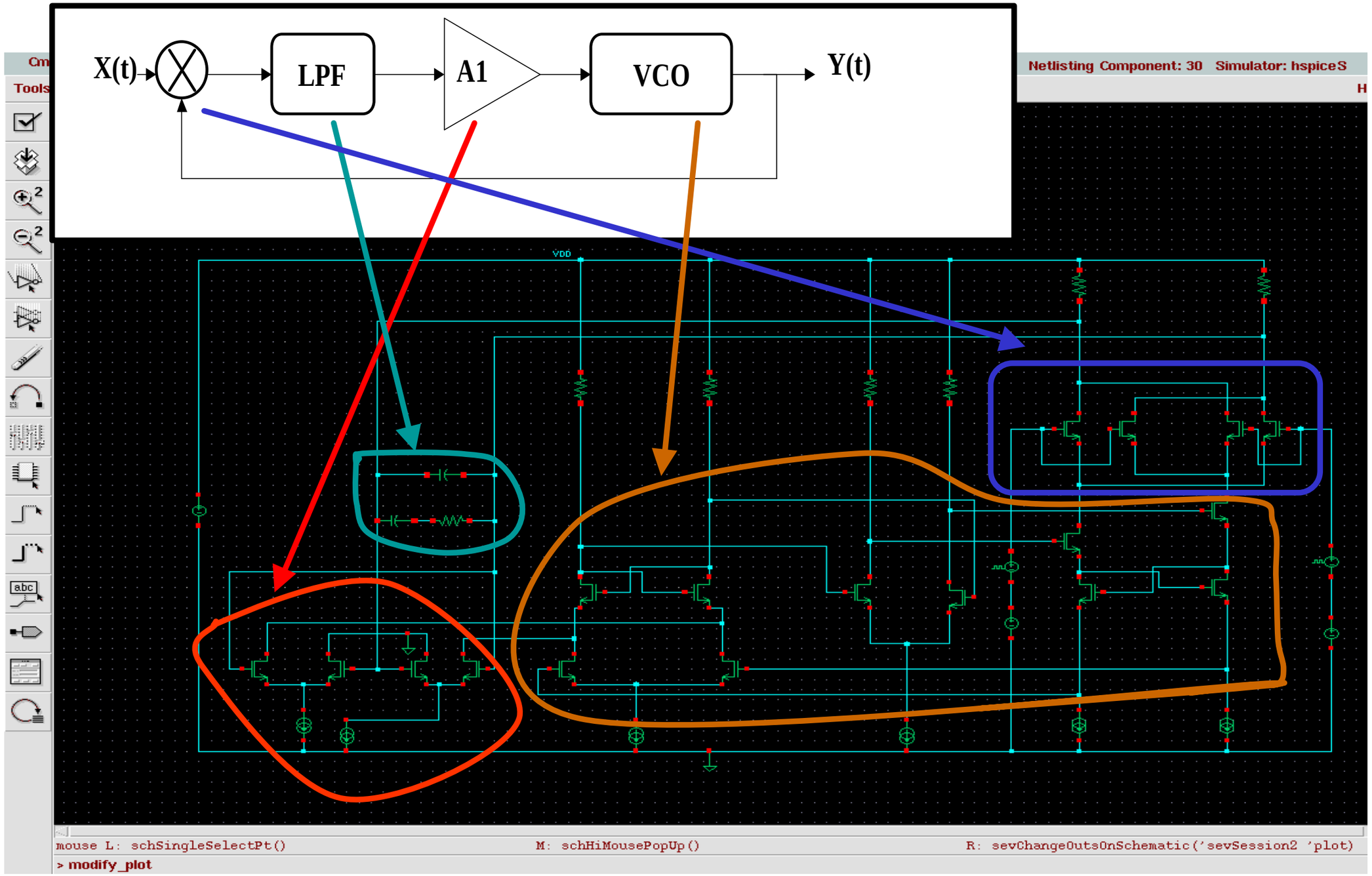




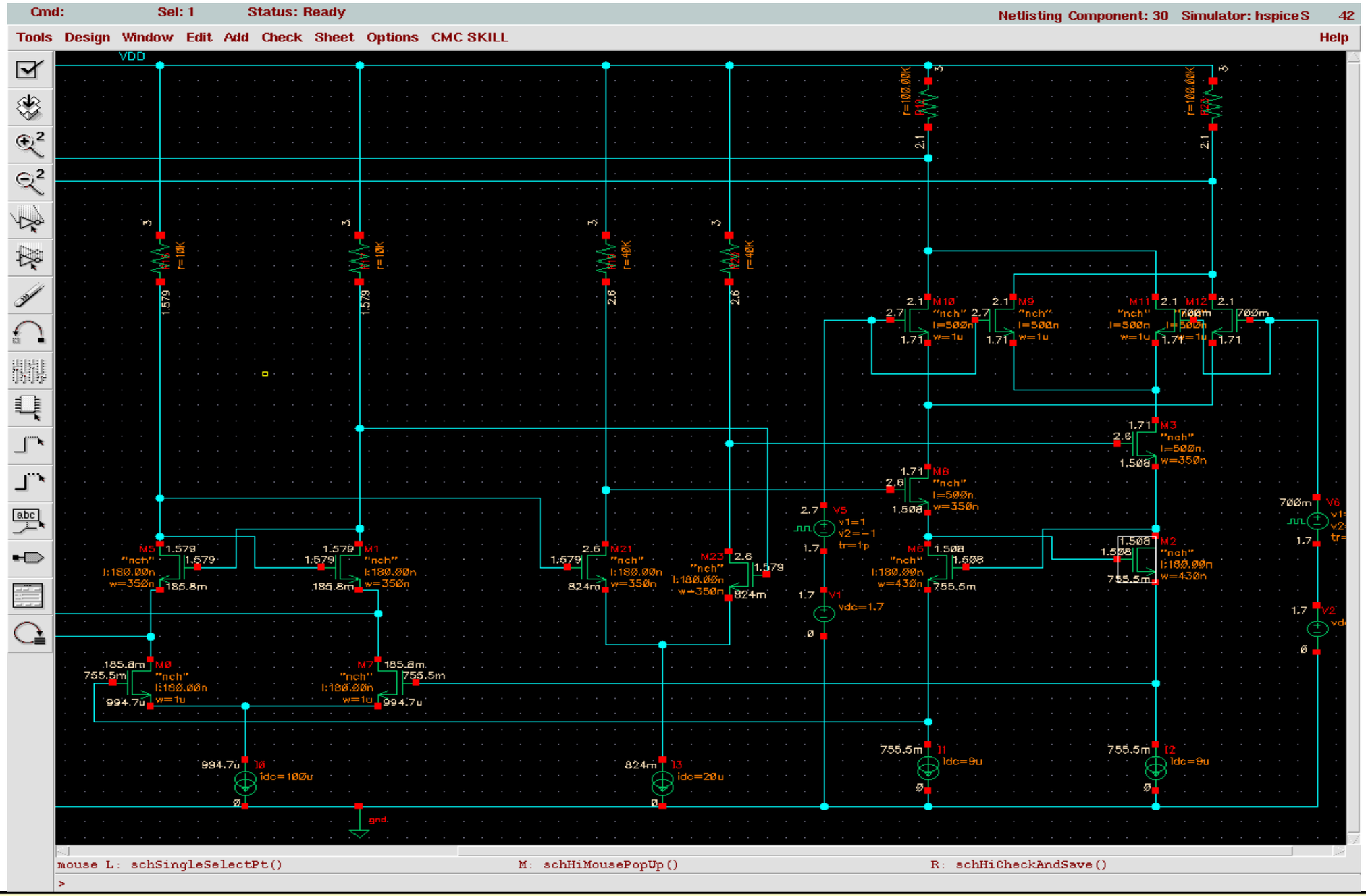
Block Diagram of Implemented 2.7 Ghz Analog Phase-Locked Loop



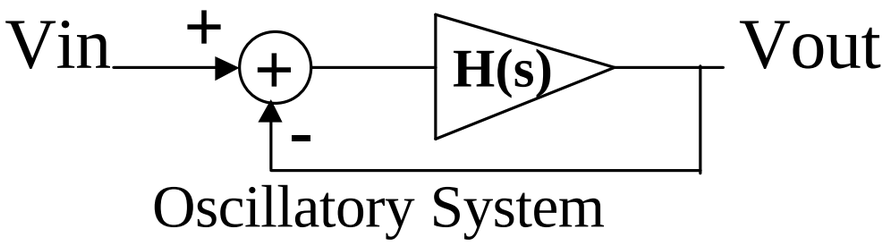
PLL Circuit Implementation



DC Analysis and Operating Points

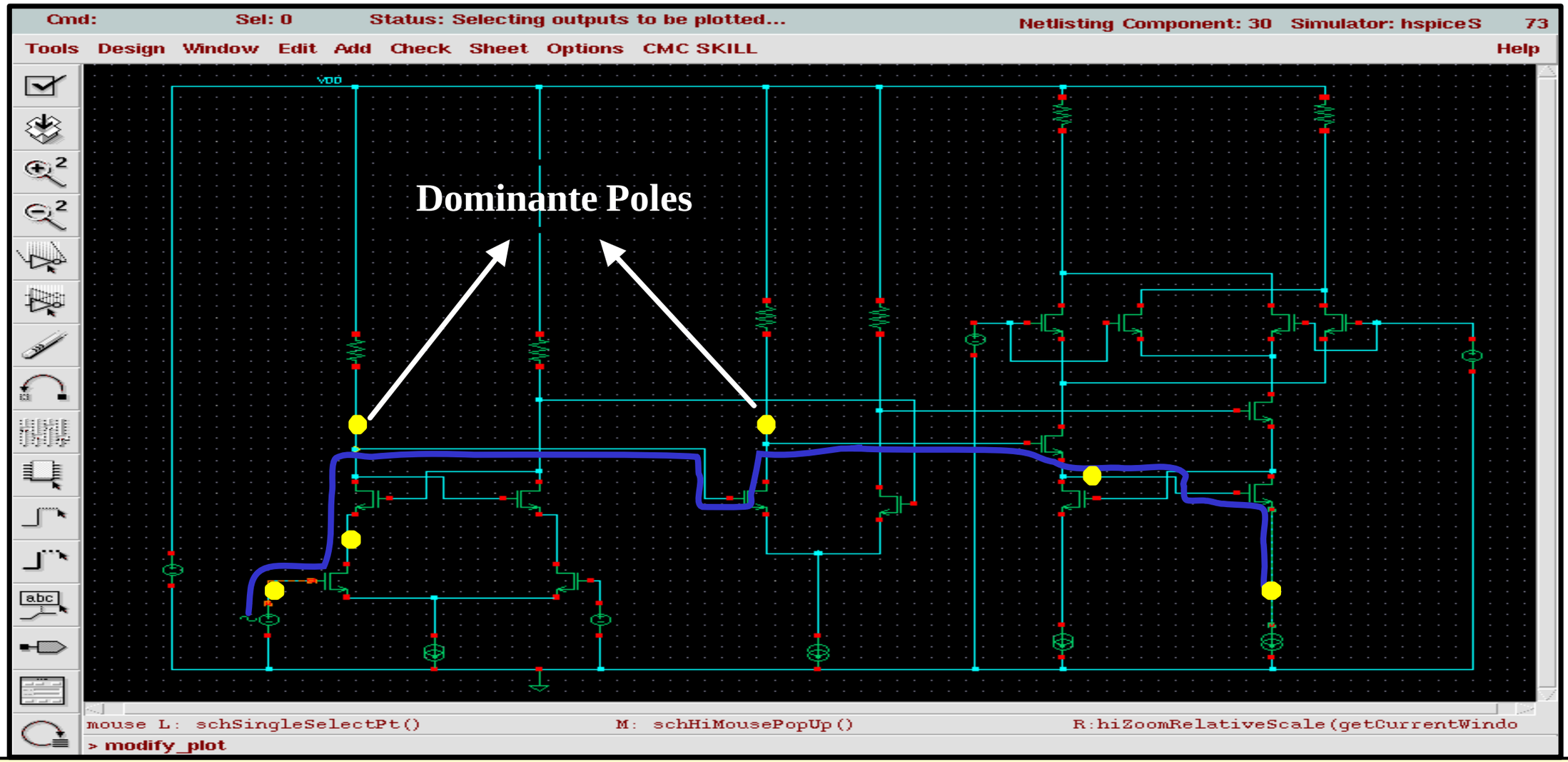


Three Stage Ring Oscillator and Mixture



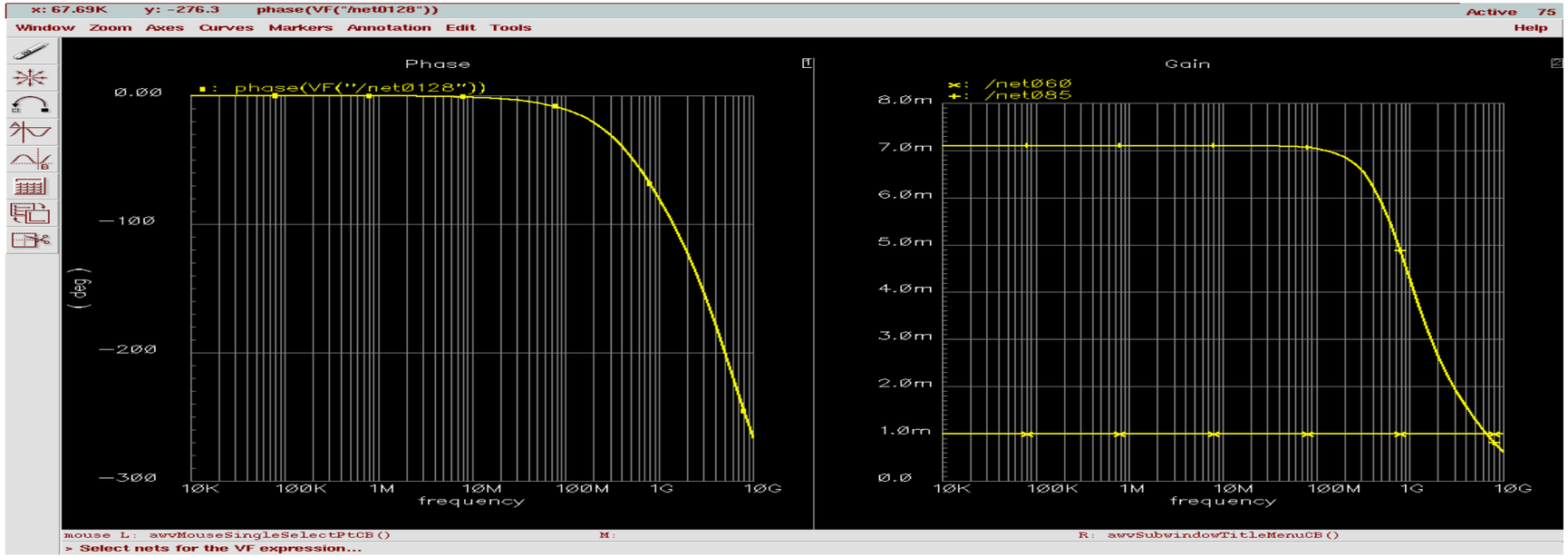
Barkhusen criteria for oscillation

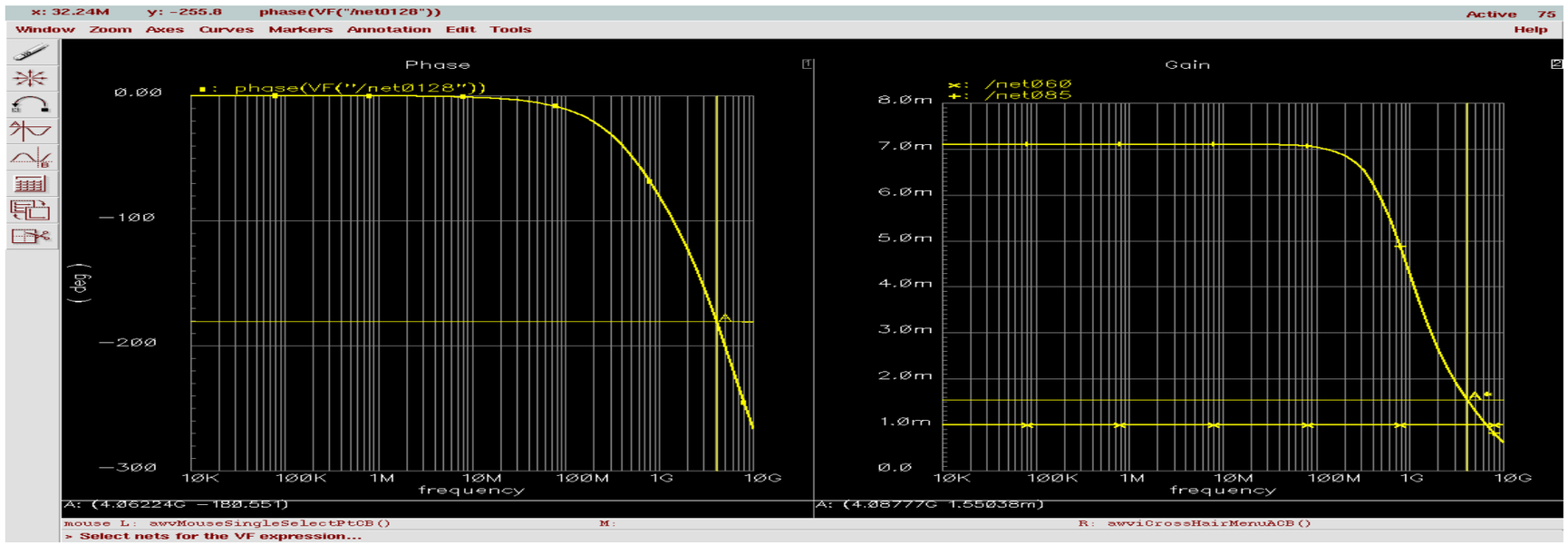
$$\begin{cases} 1- \left|H(jw)\right| \geq 1 \\ 2- \angle H(jw) \geq 180^{o} \end{cases}$$



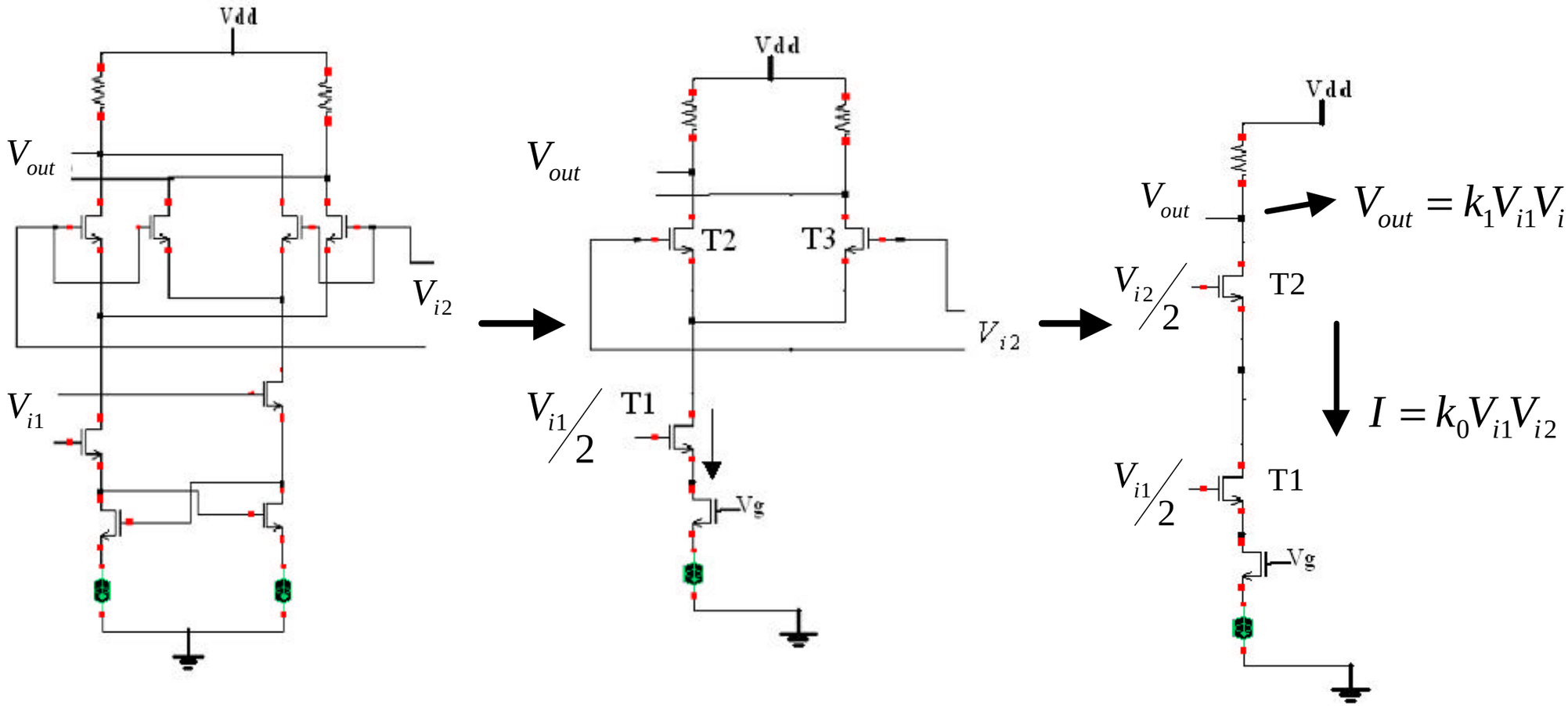
AC analysis

Bode Diagram to see if the oscillation requirements are met. To ensure oscillation in the presence of temperature and process variation gain should be more than two times of the required value





Double Balanced Mixture

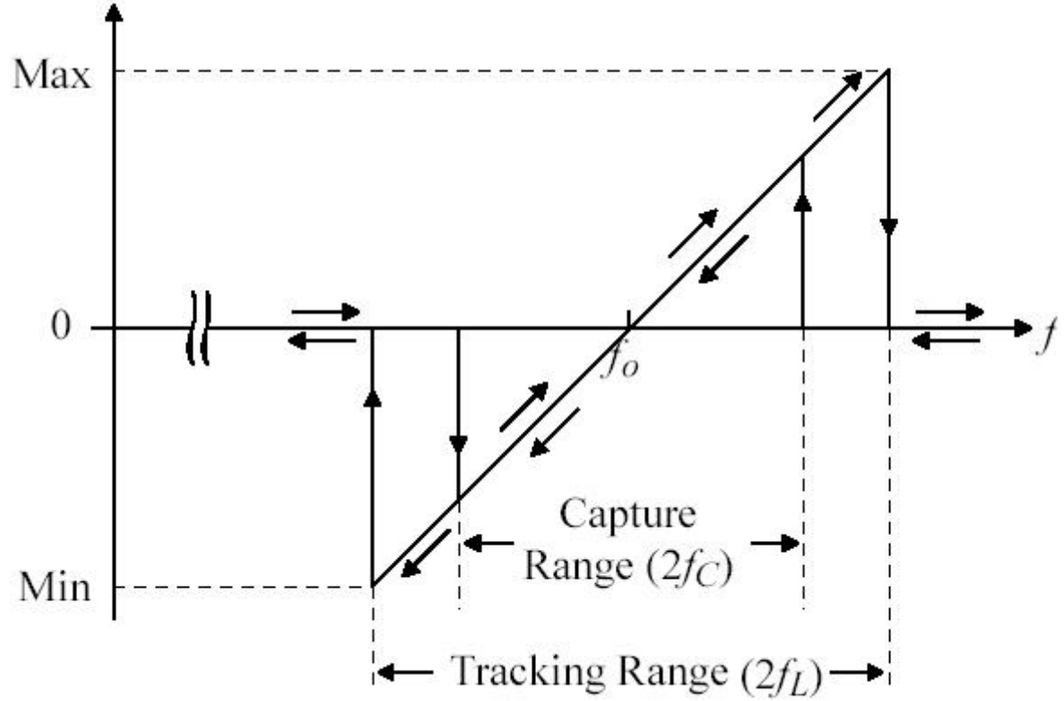


Concept of half circuit to calculate V_{out}

PLL Parameters

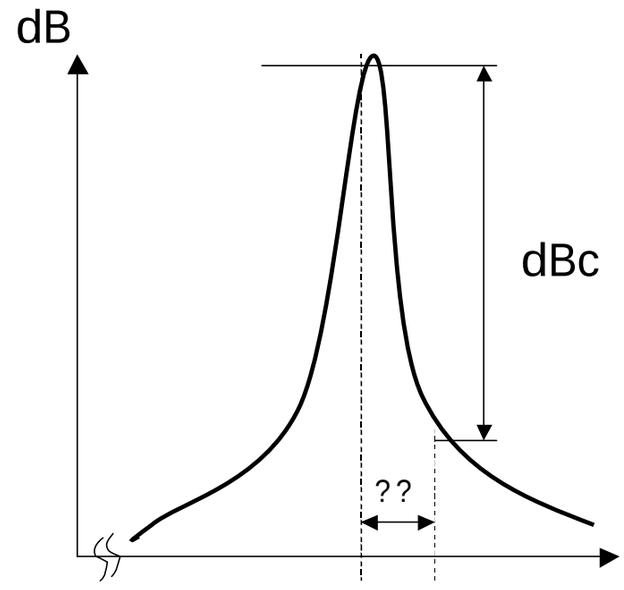
Capture Range: The capture range is the range of input frequencies for which an initially unlocked loop will lock on an input signal

Tracking Range: The range of frequencies where the PLL maintains $w_i = w_{osc}$

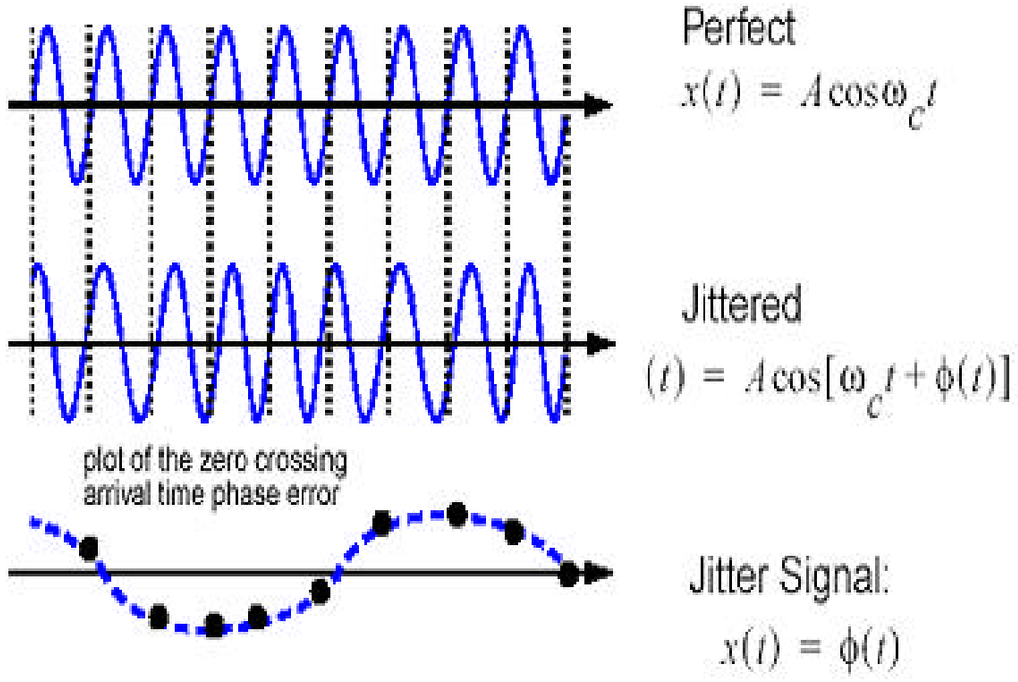


PLL Parameters

Phase noise: Represents total energy being "concentrated" close to the center frequency of operation. It is specified in FM noise (Hz rms) or dBc/Hz



Jitter: Represent the same phenomena in time domain and specified in (nsec rms) or degrees rms,



Performance of the designed PLL

Our Design

Center Frequency: 2.7 GHz
Power Dissipation: 0.960µw
Tracking Range: 120Mhz
Capture Range: 84 Mhz
Jitter: 2.6 ps, rms
Supply Voltage: 3 V
Technology: CMOS 0.18µm

Reference Design

Center Frequency: 2 GHz
Power Dissipation: 1.6µw
Tracking Range: 100MHz
Capture Range: 70 MHz
Jitter: 2.8ps,rms
Supply Voltage: 3 V
Technology: CMOS 0.6µm

References

1- **A 2-GHz 1.6-mW phase-locked loop**
*Razavi, B.;*Solid-State Circuits, IEEE Journal of , Volume: 32 , Issue: 5 , May 1997
Pages:730 – 735

2- **RF Microelectronics** Author:Behzad Razavi, Publisher: Prentice Hall, Nov.1997

3- **Fractional/Integer-N PLL Basics, Texas Instrument technical Brief SWRA029,** www.newwaveinstruments.com/resources/rf_microwave_resources/sections/phase_locked_loop_pll_design_circuit.htm

4- **A low-noise 1.6-GHz CMOS PLL with on-chip loop filter**
Parker, J.; Ray, D.;
Custom Integrated Circuits Conference, 1997., Proceedings of the IEEE 1997 , 5-8 May 1997 Pages:407 - 410